

FIG.2

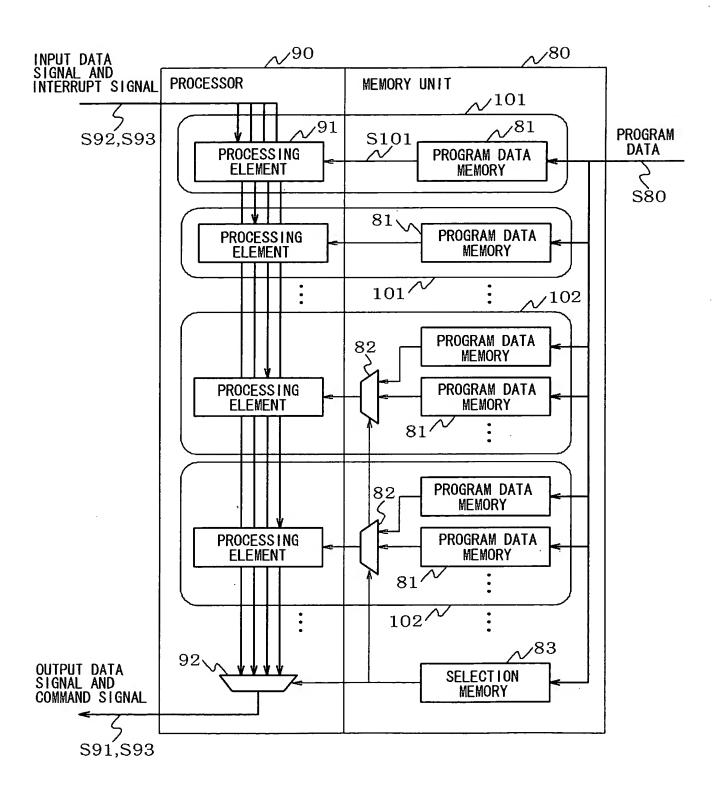


FIG.3

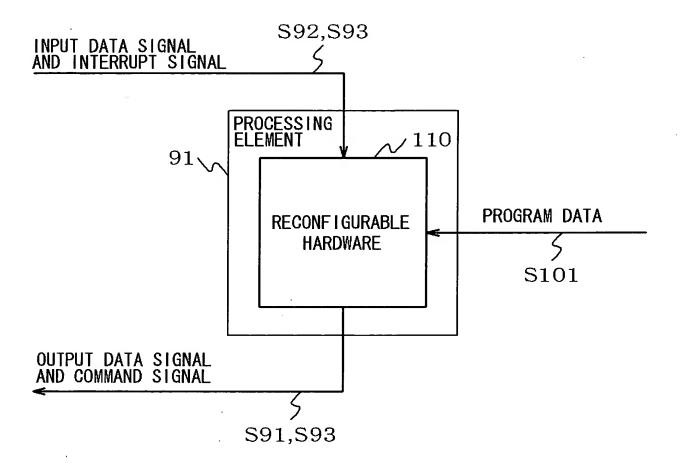
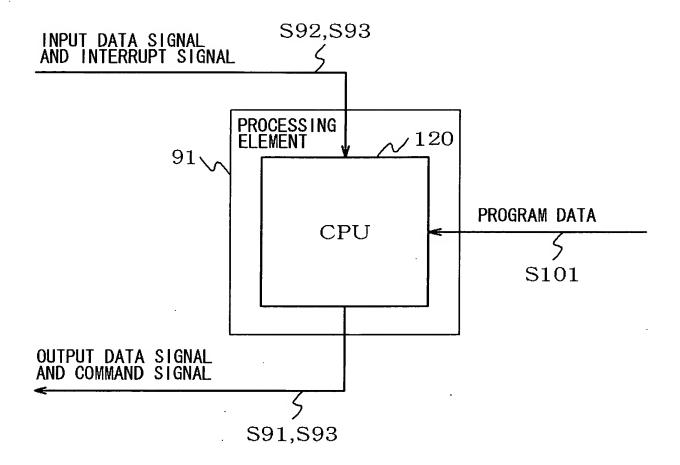
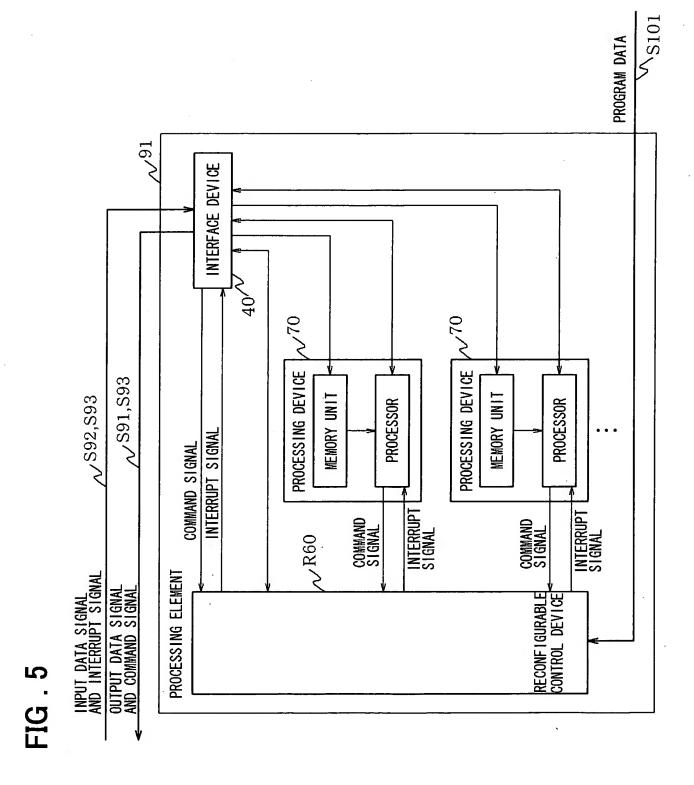


FIG . 4



Title: ELECTRONIC COMPUTER,
SEMICONDUCTOR INTEGRATED CIRCUIT,
CONTROL METHOD, PROGRAM GENERATION
METHOD, AND PROGRAM
Inventor(s): Takeshi INUO
DOCKET NO.: 029471-0194



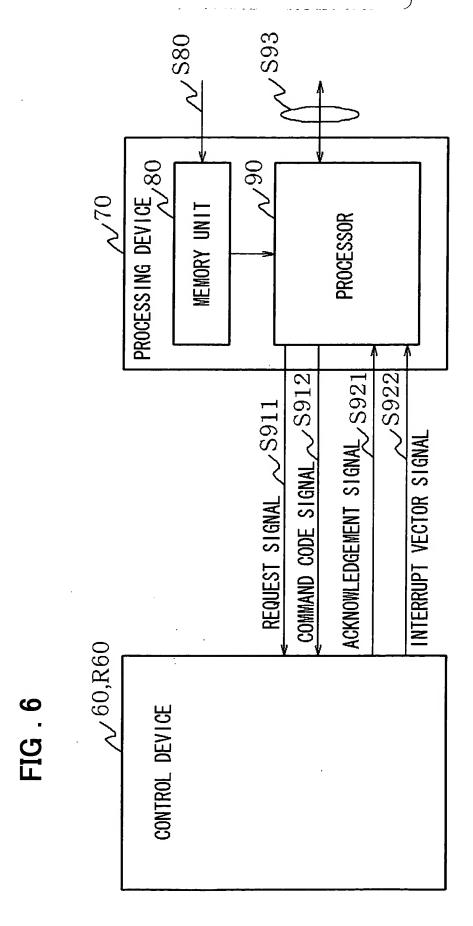


FIG . 7

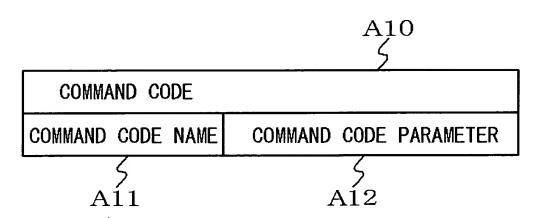


FIG. 8

CANCELS A TRANSFER OF A PROGRAM DATA STORED IN A SPECIFIED MEMORY REGION TO A REGION OF A SPECIFIED PROGRAM DATA MEMORY HALTS A OPERATION OF A SPECIFIED PROCESSING DEVICE TRANSFERS A PROGRAM DATA STORED IN A SPECIFIED MEMORY REGION TO A REGION OF A SPECIFIED PROGRAM DATA MEMORY PROGRAM DATA STORED A REGION OF A IS COMPLETE ISSUES A SPECIFIED INTERRUPT VECTOR NUMBER TO A SPECIFIED PROCESSING DEVICE SELECTS A SPECIFIED PROCESSING ELEMENT STARTS A OPERATION PROGRAM DATA MEMORY CONTENTS A SPECIFIED MEMORY REGION TO OF PROGRAM DATA MEMORY AND REGION WHERE PROGRAM DATA IS OF PROGRAM DATA MEMORY AND REGION WHERE PROGRAM DATA IS OF PROGRAM DATA MEMORY AND REGION WHERE PROGRAM DATA IS PROCESSING DEVICE AND INTERRUPT VECTOR NUMBER COMMAND CODE PARAMETER PROCESSING ELEMENT PROCESSING DEVICE REGION MEMORY I STORED REGION MEMORY STORED REGION MEMORY STORED COMMAND CODE NAME cancel_prg Interrupt wait_prg activate load_prg halt

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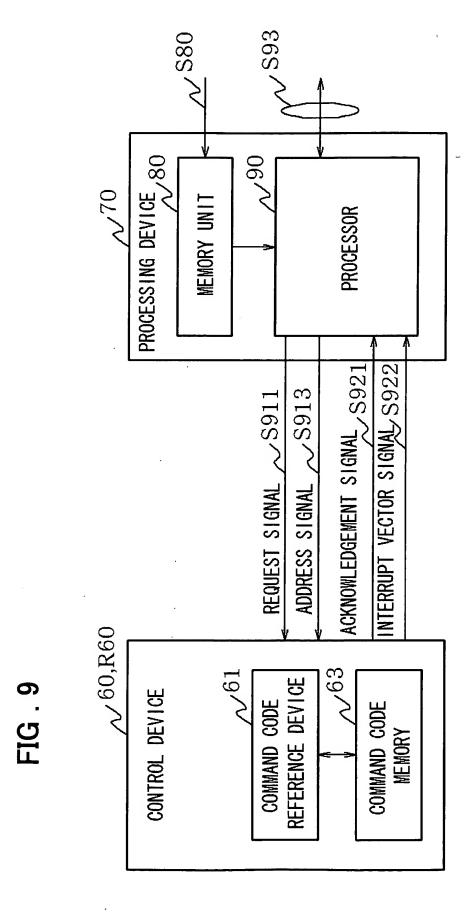


FIG . 10

ADDRESS	DATA
ADDRESS 1	COMMAND CODE 1
ADDRESS 2	COMMAND CODE 2
	: A10

S93

,S80

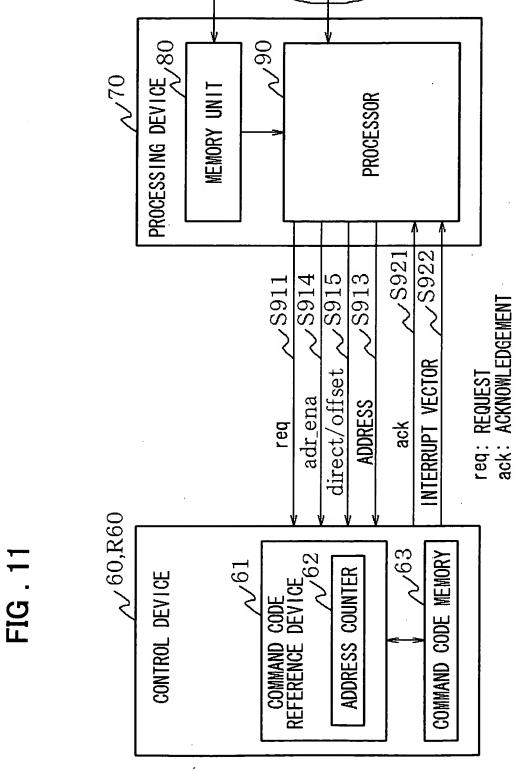


FIG . 12

ADDRESS		DATA											
ADDRESS 1	ADDRESS COUNTER	CONTROL CODE 1	FLAG 1	COMMAND CODE 1									
ADDRESS 2	ADDRESS COUNTER	CONTROL CODE 2	FLAG 2	COMMAND CODE 2									
	A20	•	A30	A10									

FIG . 13

A 20

	A20
ADDRESS COUNTER CONTROL CODE	
ADDRESS COUNTER CONTROL CODE NAME	ADDRESS COUNTER CONTROL CODE PARAMETER
A21	A22

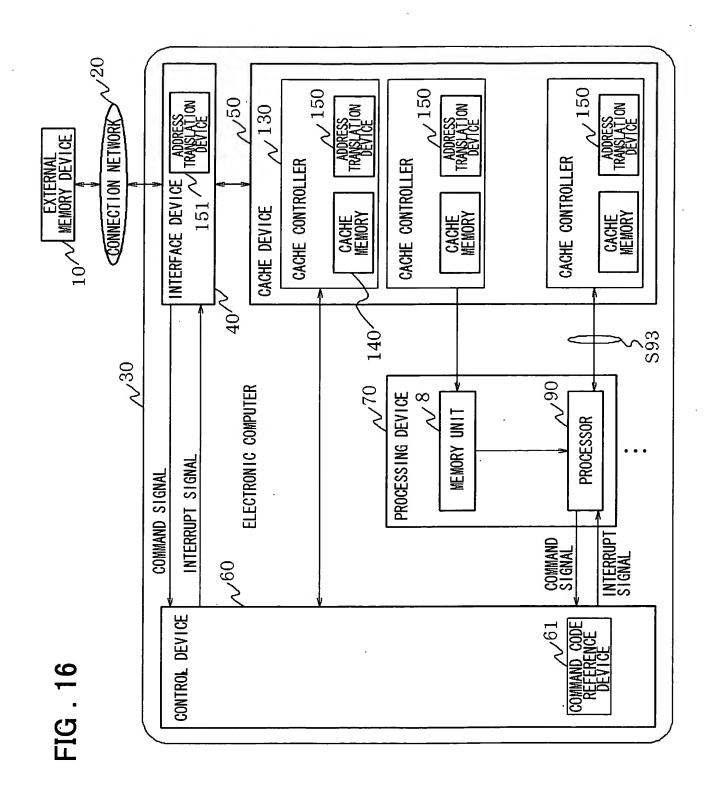
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ADDRESS COUNTER CONTROL CODE NAME	ADDRESS COUNTER CONTROL CODE PARAMETER	CONTENTS
load_adr	Z	SETS N AS THE VALUE OF THE ADDRESS COUNTER
add_adr	Z	ADDS N TO THE VALUE OF THE ADDRESS COUNTER
push_adr	N	HIDES THE VALUE OF THE ADDRESS COUNTER IN THE ADDRESS COUNTER STACK AND SETS N AS A NEW VALUE
pop_adr		RETURNS THE VALUE OF THE ADDRESS COUNTER FROM THE ADDRESS COUNTER STACK

N: NUMERICAL VALUE

FIG .15

4DDDE00	DATA	
ADDRESS	ADDRESS COUNTER CONTROL CODE AND FLAG	COMMAND CODE
:	×X100 :	✓ Y100
100	add_adr 1 cont	COMMAND CODE 100
101	load_adr 200 cont	COMMAND CODE 101
•	X200 : X101 Y	Y101 200 V
200	add_adr 1 stop	COMMAND CODE 100
201	ADDRESS COUNTER CONTROL CODE 201	COMMAND CODE 101
•	•	



Title: ELECTRONIC COMPUTER, SEMICONDUCTOR INTEGRATED CIRCUIT, CONTROL METHOD, PROGRAM GENERATION METHOD, AND PROGRAM

Inventor(s): Takeshi INUO DOCKET NO.: 029471-0194

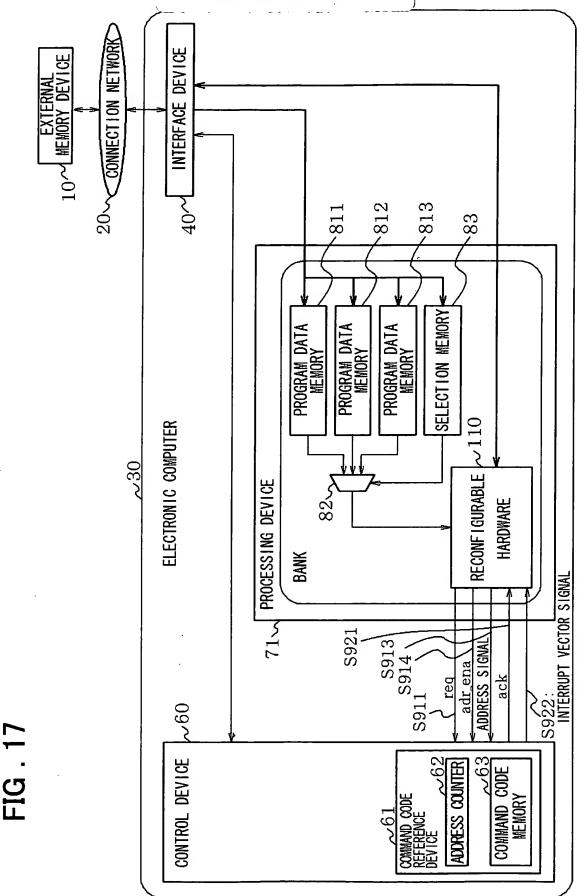


FIG. 18

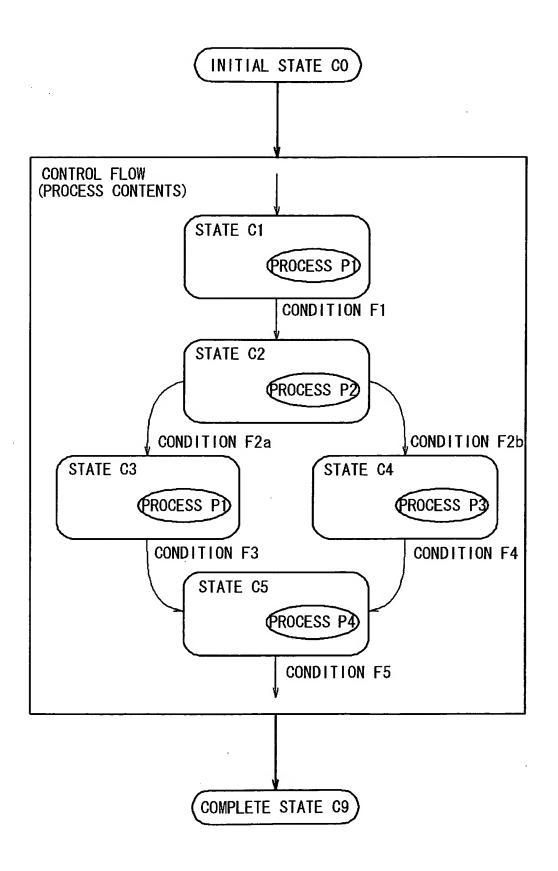
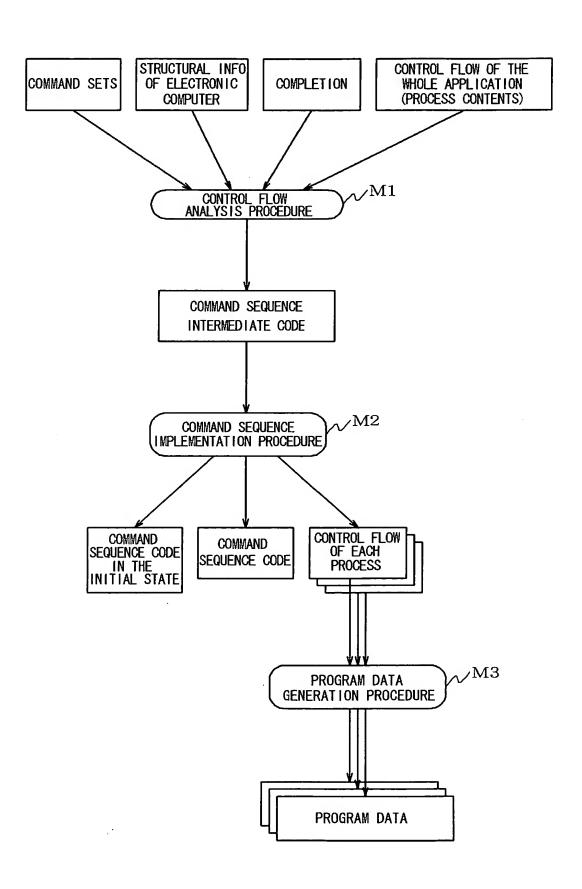
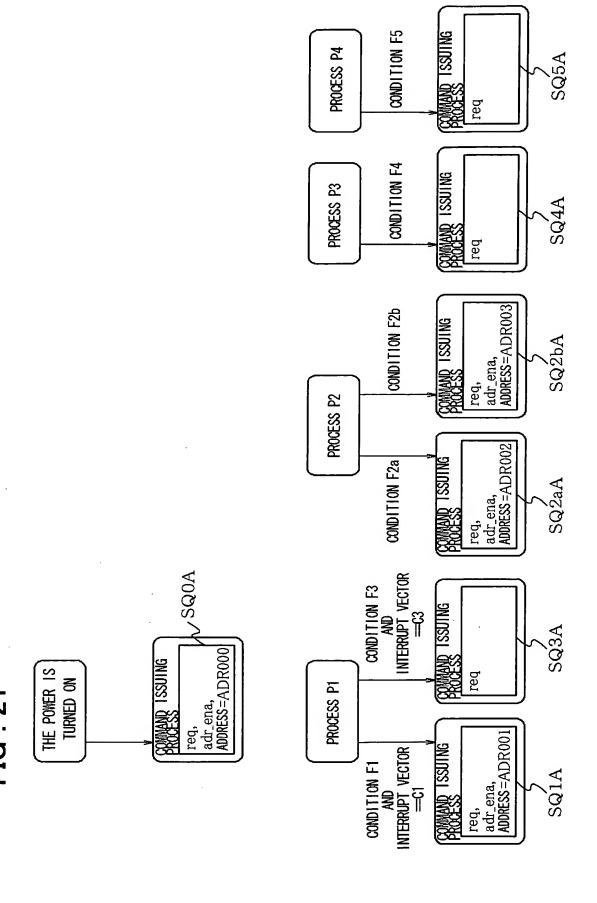


FIG . 19



	N SQ0	$ m \sim$ SQ1	V SQ3	\sim SQ2 a	\sim SQ2b	V SQ4	\sim SQ5
COMMAND SEQUENCE INTERMEDIATE CODE	load_prg 812, PM1 wait_prg 812, PM1 interrupt 71, C1 activate 812 load_prg 813, PM2	prg 813, PM2 /ate 813 prg 811, PM3	prg 813, PM4/ate 813	cancel.prg 811, PM3 interrupt 71, C3 activate 812 load.prg 813, PM4	prg 811, PM3 /ate 811 prg 813, PM4	prg 813, PM4 /ate 813	71
	load_prg wait_prg interrupt activate load_prg	wait_prg activate load_prg	wait_prg activate	cancel_p interrup activate load_prg	wait_prg activate load_prg	wait_prg activate	halt
PROGRAM DATA MEMORY USED	811	812		813		811	813
01 S	111	1+1				1.1	8
MOVES TO	STATE C1	STATE C2	STATE C5	STATE C3	STATE C4	STATE C5	COMPLETION STATE C9
TRANSITION CONDITION MOVE	STATI C1	CONDITION FI STATE AND INTERRUPT VECTOR=C1 C2	CONDITION F3 AND AND C5 INTERRUPT VECTOR==C3	CONDITION STATE F2a C3	CONDITION STATE F2b C4	CONDITION STATE F4 C5	CONDITION COMPLET STATE F5 C9
	INITIAL — STATE C1				CONDITION F2b	·	·



IG . 22

			008				0	V 3&1		,	\sim SQ2a			, SO 9b	V 2821			√ SQ3,SQ4		/ SQ5	
		PM1	PM1	C1		PM2	PM2		PM3	PM3	C3		PM4	PM3		PM4	DNA	1 141 1			
	COMMAND CODE	812,	812,	71,	812	813,	813,	813	811,	811,	71,	812	813,	811,	811	813,	813	813		71	
COMMAND SEQUENCE	COMMA	load_prg	wait_prg	interrupt	activate	load_prg	wait_prg	activate	load_prg	cancel_prg	interrupt	activate	load_prg	wait_prg	activate	load_prg	wait nro	activate		halt	
COMMAND	OL CODE	cont	cont	cont	cont	stop	cont	cont	stop	cont	cont	cont	stop	cont	cont	stop	cont	stop	1	stop	
	ADDRESS COUNTER CONTROL CODE	add_adr 1	add_adr 1	add_adr 1	add_adr 1	add_adr 0	add_adr 1	add_adr 1	add_adr 0	add_adr 1	add_adr 1	add_adr 1	load_adr ADR004	add_adr 1	add_adr 1	load_adr ADR004	add adr 1	add_adr 1		add_adr 0	
OFFRET VALUE	OI OLI VALUL	0+	+1	+2	რ +	+4	0+	- +	+2	0+	+	+2	+3	0+	+1	+2	+	+		+5	
BASE ANDRESS VALUE	האטר אמשורטט זערטר	ADR000					ADR001			ADR002				ADR003			ADR004				

FIG . 23

MEMORY]
PROGRAM DATA ISSUING COMMAND FOR SQOA	√ PM0
PROGRAM DATA ISSUING COMMANDS FOR PROCESS P1, SQ1A, AND SQ3A	√PM1
PROGRAM DATA ISSUING COMMANDS FOR PROCESS P2, SQ2aA, SQ2bA	√PM2
PROGRAM DATA ISSUING COMMANDS FOR PROCESS P3, SQ4A	PM3
PROGRAM DATA ISSUING COMMANDS FOR PROCESS P4, SQ5A	PM4

FIG. 24

PMO IS STORED IN THE PROGRAM DATA MEMORY 811 THE PROGRAM DATA MEMORY 811 IS ACTIVATED

PM2 IS BEING TRANSFERRED N PM4 IS BEING TRANSFERRED THE CONTENT HELD BY THE PROGRAM DATA MEMORY 813 THE CONTENT HELD BY THE PROGRAM DATA NEMORY 812 PM1 PM3 IS BEING TRANSFERRED TRANSFER SUSPENDED THE CONTENT HELD BY THE PROGRAM DATA NEMORY 811 PM0 PM3 IS BEING TRANSFERRED TO 811 PM4 IS BEING TRANSFERRED TO 813 THE OPERATIONAL CONTENT OF CONTENT OF THE PROGRAM THE PROGRAM ELEMENT 110 DEVICE 51 PWI IS BEING THAN SFERRED TO 812 PN2 IS BEING TRANSFERRED TO 813 TRANSFER SUSPENDED (CONDITION F5) CONDITION 2a) PROCESS PO ACCESS P4 PRODESS P1 CONDITION THE CONTENT OF THE INTERRUPT VECTOR SIGNAL S922 \Box PM2 PM3 PM4 . PM2 813, PM4 PM3 812, PM 812, PM1 \mathbf{c} 813 813 req(ADR000) 813 813 812 812 813 req(ADR001) 811 7 811 req(ADR002) cancel prg interrupt load prg activate load prg load prg interrupt activate load_prg wait_prg wait_prg activate wait_prg activate red 9 THE OPERATIONAL CONTENT OF THE CONTROL DEVICE 60 halt ADR002+0 ADR002+1 ADR002+3 ADR004+0 ADR000+0 ADR000+3 ADR001+0 ADR001+2 ADR002+2 ADR004+2 THE VALUE OF THE ADDRESS COUNTER 62 ADR000+2 ADR000+4 ADR001+1 ADR000+ ADR004+1 T109 T110 T111 T123 T124 T101 T102 T103 T104 T105 T106 T112 T113 T114 T115 T116 T117 T118 T119 T120 T121 T122

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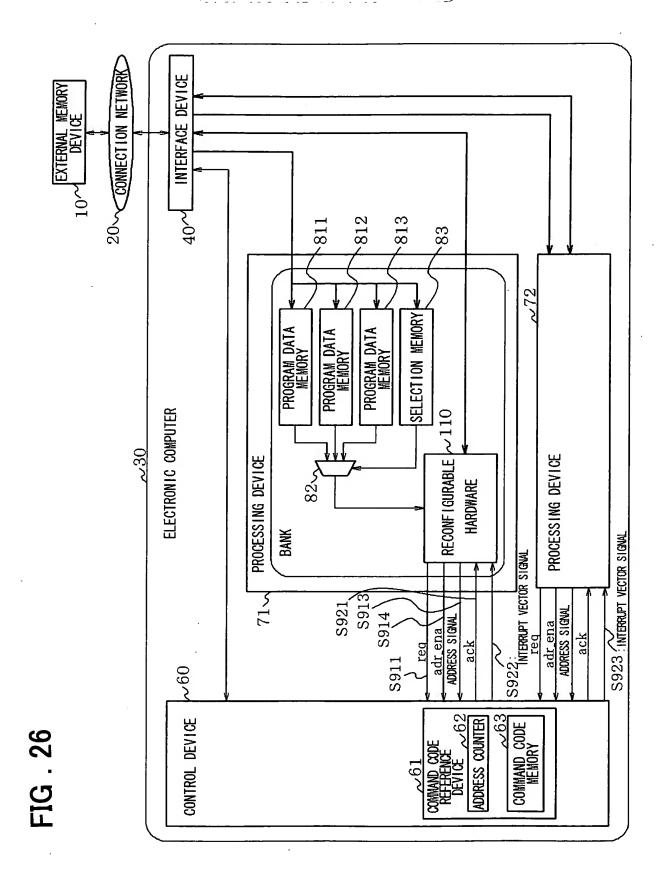


FIG . 27

			000	/ 2&0			Ç	V 541			\sim SQ2a			, sO9b	V 3820			\sim SQ3,SQ4		a 500.	√ 3&3D	
		PM1	PM1	C1		PM2	-PM2		PM3	PM3	C3		PM4	PM3		PM4	עעמ	1 IM 4			1D71	
	COMMAND CODE	812,	812,	71 ,	812	813,	813,	813	811,	811,	71 ,	812	813,	811,	811	813,	010	813		71	72,END71	
COMMAND SEQUENCE	COMINA	load_prg	wait_prg	interrupt	activate	load_prg	wait_prg	activate	load_prg	cancel_prg	interrupt	activate	load_prg	wait_prg	activate	load_prg	tions	wait_pig activate		halt	interrupt	
COMMAND	JC CODE	cont	cont	cont	cont	stop	cont	cont	stop	cont	cont	cont	stop	cont	cont	stop	+400	stop	-	cont	stop	
	ADDRESS COUNTER CONTROL CODE	add_adr 1	add_adr 1	add_adr 1	add_adr 1	add_adr 0	add_adr 1	add_adr 1	add_adr 0	add_adr 1	add_adr 1	add_adr 1	load_adr ADR004	add_adr 1	add_adr 1	load_adr ADR004	ו יוף סוף ס	add_adr 1		add_adr 1	add_adr 0	
OTTOTT VALUE	UPPISET VALUE	0+	+	+2	+3	+4	0+	+1	+2	0+	+1	+2	+3	0+	+1	+2	+	+ -		+2	+3	
BACE ADDDECS VALUE	DASE AUDRESS VALUE	ADR000					ADR001			ADR002				ADR003			ADROUG					

FIG . 28

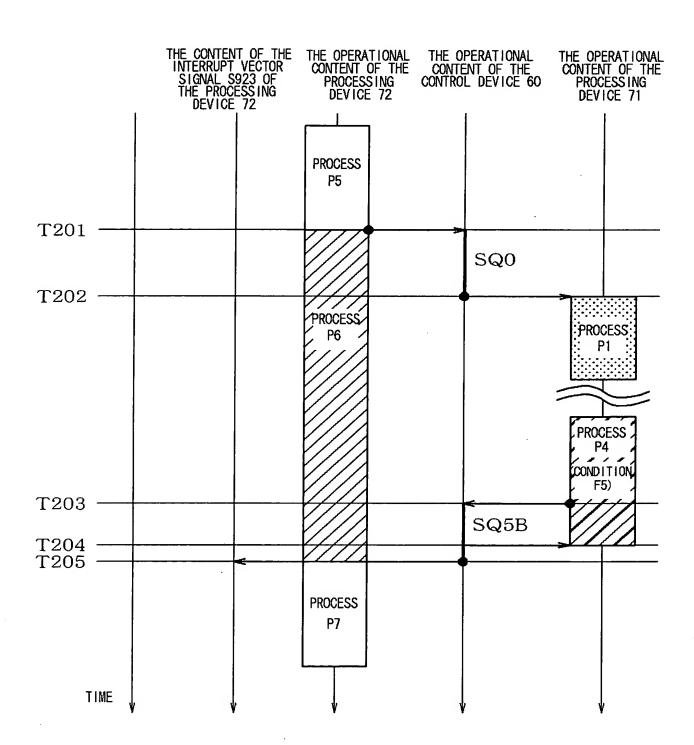


FIG. 29

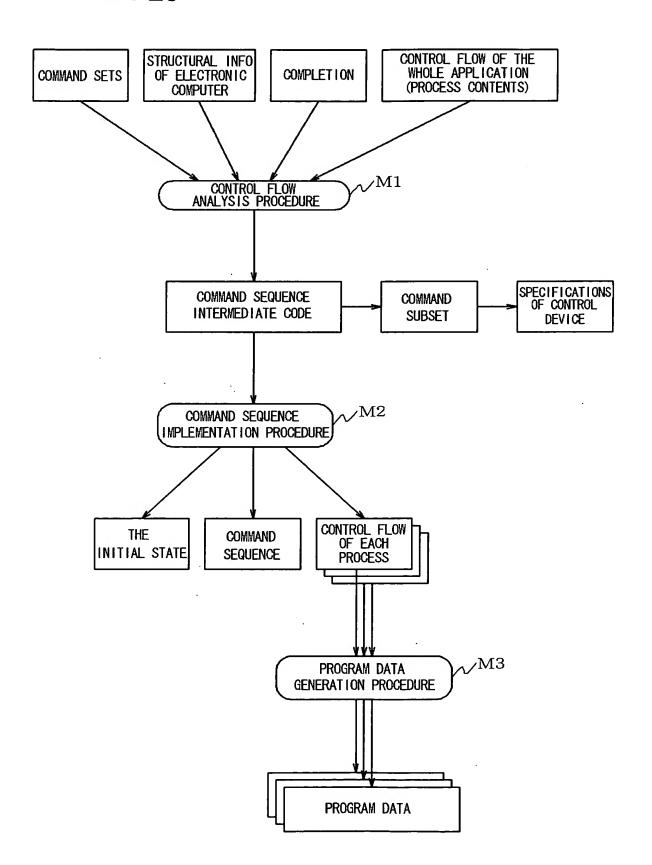


FIG . 30

PRIOR ART

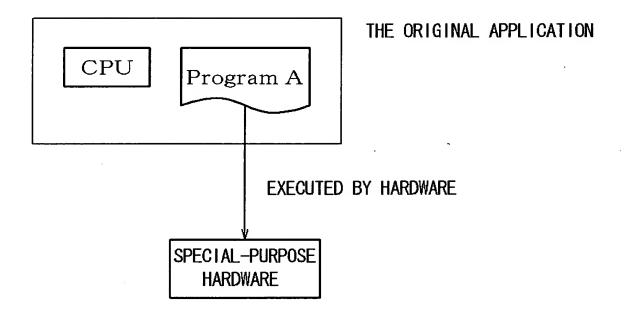


FIG . 31

PRIOR ART

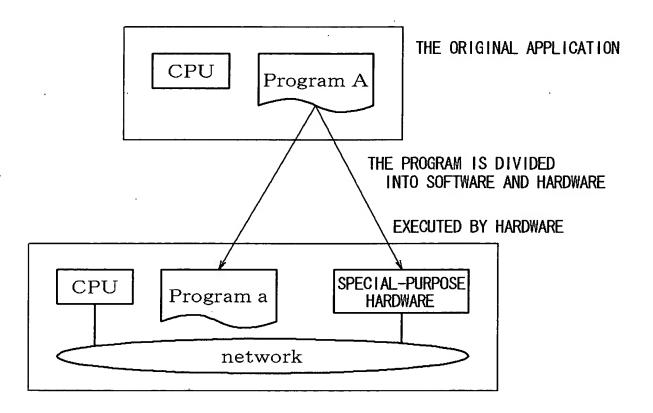


FIG . 32

PRIOR ART

